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Art Unit	2141
Examiner Name	Kristie Shingles
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ENCLOSURES *(Check all that apply)*

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  - ☐ Fee Attached
- ☐ Amendment/Reply
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  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
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Firm Name	Warn, Hoffmann, Miller & LaLone, P.C.		
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	09/785,123
Filing Date:	February 16, 2001
Applicant:	Jason Sodergren
Group Art Unit:	2141
Examiner:	Kristie Shingles
Title:	MULTI-PROTOCOL ADAPTER FOR IN-VEHICLE AND INDUSTRIAL COMMUNICATIONS NETWORK
Attorney Docket:	DEA-00002 (formerly DGI-103-A)

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APPELLANT'S SUPPLEMENTAL BRIEF

This is Appellant's Supplemental Brief being filed in response to the Notification of Non-Compliant Appeal Brief mailed April 4, 2006. Appellant's Brief filed in accordance with 37 CFR §1.192 appealing the Examiner's Final Rejection mailed January 27, 2005 was filed December 22, 2005. Appellant believes no fee is due for this Supplemental Brief.

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I. Real Party in Interest

The real party in interest for this appeal is the Dearborn Group, Inc. of Farmington Hills, Michigan, the Assignee of this application.

II. Related Appeals and Interferences

There are no related appeals or interferences.

III. Status of the Claims

Claims 1, 4-9 and 12-16 are pending in this application. Claims 2, 3, 10 and 11 have been cancelled. Claims 1, 4, 6-9 and 12-15 stand rejected under 35 USC §103(a) as being unpatentable over U.S. Patent No. 5,970,069 issued to Kumar et al. (hereinafter Kumar) in view of U.S. Patent No. 6,243,596 issued to Kikinis (hereinafter Kikinis). Claim 5 stands rejected under 35 USC §103(a) as being unpatentable over Kumar in view of Kikinis and U.S. Patent No. 6,526,335 issued to Treyz et al. (hereinafter Treyz). Claim 16 stands rejected under 35 USC §103(a) as being unpatentable over Kumar in view of Kikinis and U.S. Patent No. 5,659,471 issued to Parmee et al. (hereinafter Parmee).

IV. Status of Amendments

All amendments have been entered.

V. Summary of the Invention

Appellant's claimed invention is a multi-protocol adapter that includes an integrated CPU (figure 2) having an embedded operating system that allows the adapter to simultaneously communicate with several computers using different protocols, page

2, paragraph 4 and page 3, paragraph 2. A schematic diagram of the adaptor is shown in figure 1 and discussed on page 14, last paragraph to page 15, last paragraph. The adapter includes software interface modules 3, 4 and 5, device drivers 2, and an embedded operating system 1. Further, daughterboard interface slots are represented as memory space/I/O space /interrupt hardware interface 13 that is coupled to the device drivers 2 for connection of different daughterboard interface modules. The daughterboard interface modules are shown in figure 3. The operating system performs one or more of interrogating, monitoring, retrieving data, downloading data, recording data, revising/updating data, performing diagnostics and revising/updating the operating program of the computer, page 3, paragraph 2. The adapter also includes a plurality of daughter board interface slots, shown in figure 3, for accepting daughterboard interface modules that expand the number of protocols or change the protocols available to the adapter, page 3, paragraphs 4 and 5 and page 4, paragraph 4. Support for the various protocols that are supported by the protocol adapter can also be found on pages 11 and 12 of the specification. In one embodiment, the multi-protocol adapter has a particular application as a programmable gateway to many different types of automotive/industrial serial multiplex networks and Ethernet/connected computers and networking equipment, page 2, paragraph 1. The various multiplex networks, computers and networking equipment may be using different computer protocols, and thus are incompatible with each other, page 2, paragraph 6. The protocol adapter allows the various systems to communicate with each other over a variety of different protocols, page 2, paragraph 6.

VI. Grounds of Rejection to be Reviewed on Appeal

Whether claims 1, 4, 6-9 and 12-15 should be rejected under 35 USC §103(a) as being unpatentable over Kumar in view of Kikinis; whether claim 5 should be rejected under 35 USC §103(a) as being unpatentable over Kumar in view of Kikinis and Treyz; and whether claim 16 should be rejected under 35 USC §103(a) as being unpatentable over Kumar in view of Kikinis and Parmee et al.

VII. Argument

A. Claims 1, 4, 6-9 and 12-15 are not obvious in view of the combination of Kumar and Kikinis

1. *Prima Facie* Obviousness

MPEP 2143 states that in order to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art references must teach or suggest all of the claim limitations. Appellant submits that the Examiner has not established a *prima facie* case of obviousness because there is no suggestion or motivation in the references to combine the reference teachings, and the references do not teach or suggest all of the claim limitations as will be discussed below.

2. Independent claims 1 and 4

Independent claims 1 and 4 are recreated below:

1. A multi-protocol adapter for communicating with one or more remote computers over any one of a plurality of protocols, the adapter comprising:

an integrated CPU including an embedded operating system, said operating system including software interface modules and device drivers for one or more of interrogating, monitoring, retrieving data, downloading data, recording data, revising data and performing diagnostics over any one of the plurality of protocols, wherein the operating system is capable of simultaneously communicating with the one or more computers running different protocols; and

a plurality of daughter board interface slots for accepting at least one daughter board interface modules for expanding the protocols of the multi-protocol adapter.

4. A multi-protocol adapter for communicating with one or more remote computers over any one of a plurality of protocols, the adapter comprising:

an integrated CPU having an embedded operating system, said operating system including software interface modules and device drivers for one or more of interrogating, monitoring, retrieving data, downloading data, recording data, revising data and performing diagnostics over any one of the plurality of protocols, wherein the operating is capable of simultaneously communicating with the one or more computers running different protocols;

the CPU having simultaneous interaction between at least one multiple device using multiple protocols;

at least one daughter board having interconnect slots;

an interface for interconnection of the at least one daughterboard;

a serial port for diagnostics and system maintenance;

a flash socket for storage of system software;

a slot for connection of a peripheral;

a socket for connection of RAM;

an interface for connection of system RAM;

an interface for connection of mass-storage devices;

a battery for clock and configuration memory backup;

an infrared serial interface; and

a piezoelectric speaker.

3. Discussion of Kumar

U.S. Patent No. 5,970,069 issued to Kumar discloses a communications system that includes a remote access processor 34. The processor 34 allows various devices, such as a file server 46, a computer 38, an internet network 50, a network server 30, a personal computer 52, a video server 51, etc., to communicate with each other through local area network (LAN) interfaces 36, serial wide area network (SWAN) interfaces 40, 42 and 44, and peripheral component interfaces 38. Figure 3 is a block diagram of the remote access processor 34. Column 4, lines 39-41 state that "[R]emote access processor 34 is preferably implemented on a single semiconductor integrated circuit within network server 30."

Appellant submits that the remote access processor 34 fairly taught by Kumar is part of a server (column 4, lines 39-41) or a PC (column 5, lines 8-10) in a network system that allows various devices to communicate with each other. Appellant's protocol adapter is a stand-alone unit that is connected between two computers, such

as a computer on a vehicle and a laptop that allows the computers to talk to each other even though they are using different protocols. Further, Appellant's multi-protocol adapter allows multiple computers to simultaneously communicate with each where the computers may all be using different protocols.

Independent claims 1 and 4 state that the multi-protocol adapter can simultaneously communicate with several remote computers that are running different protocols. Appellant acknowledges that the various interfaces used by the remote access processor 34 may be operating different protocols. However, Appellant submits that Kumar does not teach or suggest that the processor 34 can simultaneously communicate with the various devices using different protocols through the interfaces.

Independent claim 1 also includes a plurality of daughterboard interface slots that accept at least one daughterboard interface module for expanding the number of protocols usable by the adapter. This feature of Appellant's invention allows the protocols supported by the adapter to be changed or increased by adding more daughterboard interface modules or exchanging one daughterboard interface module with another. In the Advisory Action, the Examiner has directed Appellant's attention to column 5, lines 8-12; column 9, lines 49-56 and column 35, lines 3-14 to teach this feature of Appellant's claimed invention. These sections of Kumar are recreated below.

> In alternative embodiments, remote access processor 34 can be located within PC 52 or portable PC 53 to provide LAN and WAN port expansion, which allows connectivity to a diverse set of network interfaces. In FIG. 2b, remote access processor 34 is implemented within an edge router 63.
>
> The RAP provides wide area connectivity to an ethernet LAN, as illustrated in FIG. 2. Up to four WAN ports are supported. WAN technologies and protocols include analog

> V.34, Basic Rate ISDN, fractional or full DS-1/E1, ADSL, cable modem or other high speed technologies up to the STS-1data rate of 52 Mbps. A PCI interface is provided for server based applications and LAN/WAN port expansion.
>
> The remote access processor of the present invention provides a robust programmable platform which enables users to install a variety of network layer protocols and internet/intrainet applications. The remote access processor platform can support popular real time operating systems such as pSOS, VxWORKS, JavaOS, and LYNX and signaling software such as Q.931 and Java Virtual Machine. In addition, these applications are supported on the samne processor as the V.34 digital signal processing software. In an alternative embodiment, the remote access processor can be integrated at the board level by assembling components from different vendors.

Appellant respectfully submits that these sections, or any other section, of Kumar does not teach a daughterboard interface module, or a plurality of daughterboard interface slots for accepting daughterboard interface modules. Appellant submits that the ability to expand LAN and WAN ports is not the same thing as providing daughterboard interface slots and daughterboard interface modules within the remote access processor 34. Column 5, lines 8-10 states that the remote access processor 34 can be put in the PC 52 or 53 as a way of expanding the LAN and WAN ports of the PCs 52 and 53. In other words, it is the processor 34 itself that is expanding the ports. Kumar does not teach that the protocols used by the processor 34 can be changed or increased as is done within the adapter of the claimed invention.

Appellant submits that once the remote access processor 34 is fabricated and packaged, it cannot be changed by adding or removing daughterboard interface modules to change the available protocols. Particularly, column 5, lines 18 – 24 states that the remote access processor 34 is implemented on a single integrated circuit chip

having a plurality of inputs and outputs. Further, the integrated circuit chip is manufactured using CMOS fabrication technology, and packaged with a 256 position plastic ball grid having the dimensions 27 mm x 27 mm x 2.1 mm. Appellant submits that it is impossible to replace or expand daughterboard interface modules in the packaged integrated circuit chip processor 34 fairly taught and suggested by Kumar because the processor 34 is a small sealed integrated chip that is not designed for this capability. All of the elements and components of the processor 34 are fixed, and cannot be replaced or added to. Therefore, Appellant submits that Kumar does not teach or suggest the daughterboard interface module or the daughterboard slots of Appellant's independent claims.

Further, independent claim 4 includes at least one daughterboard and an interface connection of the at least one daughterboard in combination with many other elements of the adapter. As discussed above, the remote access processor 34 does not include a daughterboard. Appellant submits that Kumar does not fairly teach or suggest a daughterboard interface module in a multi-protocol adapter in combination with all of a serial port with diagnostics and system maintenance, a flash socket for storage of system software, a slot for connection of a peripheral, a socket for a connection of RAM, an interface for connection of system RAM, an interface for connection of mass-storage devices, a battery for clock and configuration memory backup, an infrared serial interface and a piezoelectric speaker.

4. Discussion of Kikinis

U.S. Patent No. 6,243,596 issued to Kikinis discloses a battery pack for a cellular telephone, and has nothing to do with a multi-protocol adapter in communication with

one or more remote computers using a plurality of different protocols. It is believed that the Examiner is relying on Kikinis to teach an infrared serial interface. However, Kikinis does not teach or suggest an infrared serial interface in combination with a multi-protocol adapter of the type claimed by Appellant. Therefore, Appellant submits that the Examiner has improperly combined the teachings of Kikinis and Kumar et al. in that there is no suggestion or motivation to combine the reference teachings. Further, Kikinis does not teach or suggest an adapter simultaneously communicating with one or more computers running different protocols, and daughterboard interface slots and daughterboard interface modules for expanding the protocols of the adapter, as discussed above. Therefore, Appellant submits that Kikinis does not provide the teaching missing from Kumar et al. that would make Appellant's claimed invention obvious.

5. Dependent claims 6 – 9 and 12 – 15

Dependent claim 6 depends from independent claim 1 and states that the adapter further includes a means for defining communication routines between the adapter and a client via a host device and means for communicating between the adapter and the client after definition of communication routines between the adapter and the client. In the Advisory Action, the Examiner has directed Appellant's attention to column 4, lines 19 – 44 and column 6, line 56 – column 7, line10 to teach this feature of Appellant's invention. These sections of Kumar are recreated below:

> FIG. 1 is a block diagram of a communication system in which the present invention is useful. The remote access processor of the present invention provides connectivity from end users 10 to a variety of destinations 12 over a

communications network 14. The end users 10 can include a stand alone personal computer (PC), a stand alone work station or several PCs or work stations on a local area network (LAN). These devices can be located in a corporate branch office 16, a small business office or school 18, a home office 20 or a mobile office (e.g. hotel or auto) 22. The destinations 12 include a corporate headquarter LAN 24, an internet service provider 26 or a peer location 28, for example. Communication network 14 includes an internet or intranet connection, for example.

FIG. 2a is a block diagram illustrating a particular application of the remote access processor of the present invention which provides diverse connectivity to a network server 30 at a corporate headquarter or ISP server site. Remote access processor 34 includes local area network (LAN) interface 36, peripheral component interface (PCI) 38, and a plurality of serial wide area network (SWAN) interfaces 40, 42 and 44. Remote access processor 34 is preferably implemented on a single semiconductor integrated circuit within network server 30. PCI interface 38 allows communication between remote access processor 34 and the host processor within network server 30.

Memory controller 110 is coupled between local memory interface 66 and internal transfer bus 86. Memory controller 110 is also coupled to DMA controller and bridge circuit 112. Memory controller 110 is an integrated memory controller for supporting various local peripheral memory devices, such as a 32-bit SDRAM or an 8-bit PROM, which may be coupled to local memory interface 66. DMA controller and bridge circuit 112 is coupled between memory controller 110 and PCI interface circuit 114, and has data, address and control buses coupled to internal transfer bus 86. Circuit 112 transfers data packets between PCI interface 114 and local memory, through memory controller 110 and under the control of CPU 90. PCI interface circuit 114 is coupled between PCI interface 38 and internal transfer bus 86. PCI interface 114 is a 33 Mhz, 32-bit (3.3 Volt/5.0 Volt) interface which allows connection to external devices such as a host processor, additional LAN and WAN ports, multiple remote access processors, or network servers, for example. Finally, general purpose interrupt and control circuit 116 is coupled between interrupt and control interface 70 and internal transfer bus 86. In one embodiment, circuit 116 includes

> twelve programmable, bidirectional pins for serving additional interrupt inputs or control outputs.

Appellant respectfully submits that there is no teaching in these sections of Kumar of a multi-protocol adapter that includes an operating system capable of simultaneously communicating with one or more computers running different protocols, and includes a plurality of daughterboard interface slots for accepting at least one daughterboard interface module for expanding the protocols, where the operating system includes a technique for defining communication routines between the adapter and a host device.

Dependent claim 7 depends from independent claim 1 and states that the adapter further includes a TCP/IP connection established between two software elements, the connection of serial multiplex network messages between software entities being generalized without knowledge of a special type of multiplex network. In the Advisory Action, the Examiner directed Appellant's attention to column 4, lines 45-52; column 5, lines 47-65; column 6, lines 31-38; and column 27, lines 36-62 to teach this feature of Appellant's claimed invention. Those sections of Kumar are recreated below:

> LAN interface 36 can be configured to support a variety of protocols, such as IP and IPX over Ethernet. In the embodiment shown in FIG. 2, LAN interface 36 is an Ethernet interface which supports 10 Mb/s and 100 Mb/s data transfer rates in either full or half-duplex mode according to IEEE standards 802.3 and 802.3u. LAN interface 36 is coupled to a file server 46 and a compute server 38, for example, over Ethernet network 50.

Multi-protocol SWAN controllers 76a, 76b, 76c and 76d support four multi-protocol WAN interfaces. SWAN controller 76a is coupled directly to multi-protocol serial WAN interface 40 and is coupled to TDM serial interfaces 42a and 42b through 4-to-1 time slot multiplexers 78a and 78b. SWAN controller 76a can support a Frame Relay protocol over a leased line that is coupled to Multi-protocol WAN interface 40, for example. SWAN controllers 76b, 76c and 76d are coupled to TDM serial interfaces 42a and 42b through time slot multiplexers 78a and 78b. Time slot multiplexers 78a and 78b provide independent transmit and receive TDM interfaces at data rates of up to 8 Mhz, for example. These interfaces support ISDN, IOM2, IDL, Mitel ST-Bus, AT&T P7270 and T1/E1 communication applications, for example. Four-bit serial controller 80 is coupled to SPI interface 55 for providing synchronous, a bidirectional serial peripheral interface control for external ISDN transceivers coupled to TDM serial interfaces 42a and 42b.

CPU 90 preferably has a robust programmable platform with low level drivers and middleware to enable users to install their network layer protocols and Internet/Intranet applications. In a preferred embodiment, CPU 90 supports popular real time operating systems, such as (pSOS, VxWORKS, OS2, and LYNX), signaling software such as Q.931 and routing software such as TCP/IP.

4.7.1 Data Link Protocols

High Level Data Link Control (HDLC) links at data rates up to 52 Mbps (STS-1) are supported. HDLC framing conforms to ITU Q.921. Transmission of shared leading and trailing flags is a programmable option. Data transmission may also be paced with insertion of 0-131,072 idle characters between frames. The idle character is programmable, Either CRC-CCITT (16-bit), CRC-32 (32-bit) or no cyclic redundancy check generation/checking is selectable for bit or burst error detection.

Point to Point (PPP) Protocol packet encapsulation conforms to Internet Engineering Task Force (IETF) RFC 1549. PPP is a byte oriented synchronous protocol similar to HDLC. Frames are delimited with flag characters (7E). Control characters embedded in the PPP frames are delimited by a Control Escape (7D). This character transparency mode is

> supported on transmit and receive. Invalid frames are discarded when received.
>
> Bisynchronous communication framing conforms to International Standards Organization specifications 2111 and 1745. Sync and idle values are programmable. 16-bit Cyclic Redundancy Check (CRC-16) generation and checking are optional.
>
> Asynchronous communications is supported with the Start-Stop protocol. 7-bit or 8-bit characters with odd, even or no parity bits are selectable. Transmission of 1 or 2 stop bits is programmable.

Appellant respectfully submits that these sections of Kumar do not teach or suggest the combination of a multi-protocol adapter including an operating system that is capable of simultaneously communicating with one or more computers running different protocols, where the adapter includes a plurality of daughterboard interface slots for accepting at least one daughterboard interface module for expanding the protocols of the adapter, and a TCP/IP connection between two software elements.

Dependent claim 8 depends from independent claim 1 and states that the adapter further includes a server program handling communications between a source entity and a destination entity. In the Advisory Action, the Examiner directed Appellant's attention to column 4, line 33 – column 5, line 17, and column 34 lines 48-68 to teach this feature of Appellant's claimed invention. Those sections of Kumar are recreated below.

> FIG. 2a is a block diagram illustrating a particular application of the remote access processor of the present invention which provides diverse connectivity to a network server 30 at a corporate headquarter or ISP server site. Remote access processor 34 includes local area network (LAN) interface 36, peripheral component interface (PCI) 38, and a plurality of

serial wide area network (SWAN) interfaces 40, 42 and 44. Remote access processor 34 is preferably implemented on a single semiconductor integrated circuit within network server 30. PCI interface 38 allows communication between remote access processor 34 and the host processor within network server 30.

LAN interface 36 can be configured to support a variety of protocols, such as IP and IPX over Ethernet. In the embodiment shown in FIG. 2, LAN interface 36 is an Ethernet interface which supports 10 Mb/s and 100 Mb/s data transfer rates in either full or half-duplex mode according to IEEE standards 802.3 and 802.3u. LAN interface 36 is coupled to a file server 46 and a compute server 38, for example, over Ethernet network 50.

SWAN interfaces 40, 42 and 44 provide connectivity to remote devices 51, 52 and 53 over wide area networks 54. Remote access processor 34 provides simultaneous connectivity to all three SWAN interfaces 40, 42 and 44 from file server 46, compute server 48 and network server 30.

Device 51 includes a video server or other high speed receiver device such as a PC or a television which is coupled to SWAN interface 40 over a high speed switched digital communication link. This link can include a Frame Relay interface over a leased switched digital network or an ADSL TA interface over a public switched telephone network, for example. The Frame Relay interface transfers data at rates of 56 Kb/s to 45 Mb/s, and the ADSL interface transfers data at rates of 6-8 Mb/s with an external ADSL terminal adapter. Device 52 includes a personal computer or a work station located at a small office or home office, and is coupled to SWAN interface 42 over an Integrated Switched Digital Network-Basic Rate Interface (ISDN-BRI). The ISDN-BRI interface transfers data at a rate of 128 Kb/s. Device 53 includes a portable PC which is coupled to SWAN interface 42 or SWAN interface 44 over an ISDN-BRI or a V.34 analog network, for example.

In alternative embodiments, remote access processor 34 can be located within PC 52 or portable PC 53 to provide LAN and WAN port expansion, which allows connectivity to a diverse set of network interfaces. In FIG. 2b, remote access processor 34 is implemented within an edge router 63. LAN interface 36 is coupled to a plurality of PCs 52a-52c over

> Ethernet network 50, which allows connectivity to WAN 54 over a variety of SWAN interfaces 40, 42 and 44. Edge router 63 can be located in a stand-alone box, in network server 30 or in any one of the PCs 52a-52c.
>
> The remote access processor of the present invention can be manufactured as a low cost, high performance standard product that enables edge routers or similar edge devices for small office/home office, branch office and mobile office remote access applications. The remote access processor provides connectivity from a stand alone PC or several PCs on a local area network to a wide area network. In other embodiments, the remote access processor can be used on a remote access server at corporate headquarter site or at an internet service provider's server location. The remote access processor of the present invention supports diverse remote access technologies on a single integrated semiconductor circuit. Although the particular configurations discussed above support Ethernet, ISDN-BRI, V.34 and Frame Relay interfaces, the remote access processor of the present invention can also be configured to support ADSL, ISDN-PRI, T1/E1, T3/E3, wireless, cable modem and ATM interfaces, for example. This provides low cost connectivity with high overall performance due to low power consumption, high speed and small size. Such a structure has a high reliability since it can be manufactured with proven chip design and fabrication methodologies.

Appellant respectfully submits that these sections of Kumar do not teach or suggest a multi-protocol adapter including an operating system that is capable of simultaneously communicating with one or more computers running different protocols, and that includes a plurality of daughterboard interface slots for accepting at least one daughterboard interface module for expanding the protocols of the adapter, and a suitable program handling communications between a source entity and a destination entity.

Dependent claim 9 depends from independent claim 1 and states that the adapter further includes a message scheduler, a message responder, a message filter or a script loader. In the Advisory Action, the Examiner directed Appellant's attention to column 8, lines 40-57 and column 6, lines 50-65 to teach this feature of Appellant's invention. Those sections of Kumar are recreated below.

> When serial data is received at V.34 Codec interface 44, the data represents a sampling of the analog signal transmitted over a public switched telephone network. The sampling is performed by an external V.34 Codec (not shown) coupled to V.34 Codec interface 44. As in the case where serial data is received at one of the LAN or WAN ports DMA controller 82 collects the serial data and stores the data in local memory, through memory controller 110. Once the data samples have been stored in local memory, CPU 90 retrieves the data samples and demodulates the samples into digital data packets by performing a digital filter and data pump function through the V.34 digital signal processing algorithm. CPU 90 then stores the data packets back into local memory through memory controller 110, and notifies the routing software executed by CPU 90 to look for the packets in local memory. The routing software then retrieves the packets from local memory and determines their destination, as discussed above.
>
> Phase locked loop circuit 106 is coupled to 40 Mhz clock input 62 and provides various clock signals for sequencing the operations of remote access processor 34. Boundary scan circuit 108 is coupled to boundary scan input 64 and provides a scan test function for the various logical elements within remote access processor 34 according IEEE standard 1149.1, for example.
>
> Memory controller 110 is coupled between local memory interface 66 and internal transfer bus 86. Memory controller 110 is also coupled to DMA controller and bridge circuit 112. Memory controller 110 is an integrated memory controller for supporting various local peripheral memory devices, such as a 32-bit SDRAM or an 8-bit PROM, which may be coupled to local memory interface 66. DMA controller and bridge circuit

> 112 is coupled between memory controller 110 and PCI interface circuit 114, and has data, address and control buses coupled to internal transfer bus 86. Circuit 112 transfers data packets between PCI interface 114 and local memory, through memory controller 110 and under the control of CPU 90. PCI interface circuit 114 is coupled between PCI interface 38 and internal transfer bus 86. PCI interface 114 is a 33 Mhz, 32-bit (3.3 Volt/5.0 Volt) interface which allows connection to external devices such as a host processor, additional LAN and WAN ports, multiple remote access processors, or network servers, for example. Finally, general purpose interrupt and control circuit 116 is coupled between interrupt and control interface 70 and internal transfer bus 86.

Appellant respectfully submits that these sections of Kumar do not teach or suggest a multi-protocol including an operating system that is capable of simultaneously communicating with one or more computers running different protocols, and including a plurality of daughterboard interface slots for accepting at least one daughterboard interface module for expanding the protocols of the adapter, and a message scheduler, a message responder, a message filter or a script loader.

Dependent claims 12 – 14 depend from independent claim 1 and state that the adapter includes an on-board web server providing communications to the web. Appellant respectfully submits that Kumar does not teach an on-board web server in a multi-protocol adapter that includes an operating system capable of simultaneously communicating with one or more computers running different protocols, and including a plurality of daughterboard interface slots for accepting at least one daughterboard interface module for expanding the protocols of the adapter.

Dependent claim 15 depends from independent claim 1 and states that the plurality of protocols are selected from the group consisting of controller area network

protocols, J1850 protocols, keyboard protocol 2000 and UART-based protocols. Appellant respectfully submits that Kumar does not teach or suggest using any of these protocols in combination with the multi-protocol adapter that includes an operating system capable of simultaneously communicating with one or more computers running different protocols and a plurality of daughterboard interface slots for accepting at least one daughterboard interface module for expanding the protocols of the adapter.

B. Dependent claim 5 is not obvious in view of the combination of Kumar in view Kikinis and Treyz

U.S. Patent No. 6,526,335 issued to Treyz et al. discloses an automobile personal computer system that communicates with numerous devices and facilities, including hand-held computer devices, cellular telephones, wristwatches, laptop computers, etc., wirelessly via satellite networks. It is believed that the Examiner is relying on Treyz et al. to teach a Linux operating system. Appellant respectfully submits that there is no motivation or suggestion in Treyz et al. to combine a Linux operating system and a multi-protocol adapter. Further, Appellant submits that the Treyz et al. automobile personal computer system fails to teach or suggest an adapter simultaneously communicating with one or more computers running different protocols, and daughterboard interface slots and daughterboard interface modules for expanding the protocols of the adapter as discussed above. Therefore, Appellant submits that Kikinis does not provide the teaching missing from Kumar et al. that would make Appellant's claimed invention obvious.

C. Dependent claim 16 is not obvious in view of the combination of Kumar, Kikinis and Parmee

U.S. Patent No. 5,659,471 issued to Parmee et al. discloses a vehicular semi-automated mechanical transmission system. It is believed the Examiner is relying on Parmee et al. to teach some of the vehicle protocols identified in dependent claim 16. However, Parmee et al. does not teach or suggest an adapter simultaneously communicating with one or more computers running different protocols, and daughterboard interface slots and daughterboard interface modules for expanding the protocols of the adapter as discussed above. Therefore, Appellant submits that Parmee et al. does not provide the teaching missing from Kumar et al. that would make Appellant's claimed invention obvious.

VIII. Conclusion

Appellant respectfully submits that claims 1, 4, 6-9 and 12-15 are not obvious in view of the combination of Kumar and Kikinis, claim 5 is not obvious in view of the combination of Kumar, Kikinis and Treyz, and claim 6 is not obvious in view of the combination of Kumar, Kikinis and Parmee. It is therefore respectfully request that the Final Rejection under §103 be reversed, and that Appellant's claims be allowed.

Respectfully submitted,

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CLAIMS APPENDIX

COPY OF CLAIMS INVOLVED IN THE APPEAL

1. A multi-protocol adapter for communicating with one or more remote computers over any one of a plurality of protocols, the adapter comprising:

an integrated CPU including an embedded operating system, said operating system including software interface modules and device drivers for one or more of interrogating, monitoring, retrieving data, downloading data, recording data, revising data and performing diagnostics over any one of the plurality of protocols, wherein the operating system is capable of simultaneously communicating with the one or more computers running different protocols; and

a plurality of daughter board interface slots for accepting at least one daughter board interface modules for expanding the protocols of the multi-protocol adapter.

4. A multi-protocol adapter for communicating with one or more remote computers over any one of a plurality of protocols, the adapter comprising:

an integrated CPU having an embedded operating system, said operating system including software interface modules and device drivers for one or more of interrogating, monitoring, retrieving data, downloading data, recording data, revising data and performing diagnostics over any one of the plurality of protocols, wherein the operating is capable of simultaneously communicating with the one or more computers running different protocols;

the CPU having simultaneous interaction between at least one multiple device using multiple protocols;

at least one daughter board having interconnect slots;

an interface for interconnection of the at least one daughterboard;

a serial port for diagnostics and system maintenance;

a flash socket for storage of system software;

a slot for connection of a peripheral;

a socket for connection of RAM;

an interface for connection of system RAM;

an interface for connection of mass-storage devices;

a battery for clock and configuration memory backup;

an infrared serial interface; and

a piezoelectric speaker.

5. The multi-protocol adapter according to claim 1 wherein the embedded operating system comprises Linux operating system.

6. The multi-protocol adapter according to claim 1, the adapter further comprising:

means for defining communication routines between the adapter and a client via a host device, and

means for communicating between the adapter and the client after definition of communication routines between the adapter and the client.

7. The multi-protocol adapter according to claim 1, the adapter further comprising:

a TCP/IP connection established between two software elements, the connection of serial multiplex network messages between software entities being generalized without knowledge of a specific type of multiplex network.

8. The multi-protocol adapter according to claim 1 further comprising:

a server program handling communications between a source entity and a destination entity.

9. The multi-protocol adapter according to claim 1 further comprising:

at least one of message scheduler, a message responder, a message filter or a script loader.

12. The multi-protocol adapter according to claim 1 further comprising:

an on-board web server.

13. The multi-protocol adapter according to claim 12 further comprising:

communication between users of the adapter and the adapter via a web browser technology.

14. The multi-protocol adapter according to claim 13 further comprising communication between users of the adapter and the adapter via a web browser via HTML.

15. The multi-protocol adapter according to claim 1 wherein the plurality of protocols are selected from the group consisting of controller area network protocols, J1850 protocols, key word protocol 2000, and UART-based protocols.

16. The multi-protocol adapter according to claim 1 wherein the daughter board interface modules are selected from the group consisting of SAJ1850, UBP, CCD, SCI, CAN, SAEJ1587, J1939, J2284, J2411, ISO 11992, 9141-2 and KWP2000 modules.

EVIDENCE APPENDIX

There is no evidence pursuant to §1.130, §1.131 or §1.132.

RELATED PROCEEDINGS APPENDIX

There are no decisions rendered by a court or the Board in any proceeding identified in Section II of this Appeal Brief.